

DC TO DC CONVERTER PRODUCING OUTPUT VOLTAGE EXHIBIT RISE AND FALL CHARACTERISTICS INDEPENDENT OF LOAD THEREON

This application is a Continuation of application number 09/539,868, filed March 31, 2000, now pending, which is a divisional application of application number 08/884,082, filed June 27, 1997, now U.S. Patent 6,147,477, which is an FWC of application No. 08/757,623, filed November 27, 1996, now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power supply circuit used in various kinds of electronic apparatuses. More particularly, it relates to a circuit for controlling a direct-current to direct-current conversion so as to keep constant a voltage or voltages used in an electronic apparatus, and to a direct-current to direct-current conversion apparatus using the same. Note that, in the description below, "direct-current to direct-current conversion" is simply abbreviated as "" DC/DC "".

2. Description of the Related Art

A portable electronic apparatus such as a so-called hand-held type personal computer is equipped with a battery as its power source. Since the voltage of a battery is generally lowered as the battery discharges, a DC/DC apparatus is incorporated into the electronic apparatus so as to keep constant the output voltage of the battery.

On the other hand, the power source used in an electronic apparatus usually requires a plurality of power supplies, not a single power supply. To this end, a plurality of DC/DC apparatuses are provided for the plurality of power supplies. In this case, if turn-on/turn-off sequences between the respective power supplies are not fully taken into consideration, a drawback occurs in that a latch-up phenomenon is caused in semiconductor devices used in the electronic apparatus and thus some devices are burned out. Accordingly, some ideas are required for controlling power turn-on/turn-off sequences.

In one example of the prior art, the DC/DC

apparatus is provided with a special logic circuit for controlling such power turn-on/turn-off sequences. However, this leads to a problem in that the scale of the entire circuit becomes large and the circuit constitution also becomes relatively complicated.

Also, where respective power supplies are simultaneously turned on with respect to a plurality of DC/DC apparatuses, it is substantially impossible to control respective rise characteristics of output voltages of the DC/DC apparatuses since the rise characteristics depend on lightness or heaviness of respective loads of the DC/DC apparatuses. A similar problem also occurs in the case where respective power supplies are simultaneously turned off.

The problems encountered in the prior art will be explained later in detail in contrast with preferred embodiments of the present invention.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a DC/DC control circuit and a DC/DC apparatus using the same, by which it is possible to easily realize power turn-on/turn-off sequence controls without requiring any special logic circuit, and thus to control rise/fall characteristics of the output voltage without depending on the load.

To attain the object, the present invention is mainly characterized in that, where power turn-on/turn-off sequences are controlled between a plurality of DC/DC apparatuses (e.g., DC/DC apparatuses using a pulse width modulation (PWM) control), a plurality of reference voltages can be input to an error amplifier for voltage control provided in each DC/DC apparatus, and the rise characteristics of an output voltage obtained when the power supply to each DC/DC apparatus is turned on do not depend on the corresponding load.

Namely, the present invention is directed to devising the form of connection of a capacitor circuit for use in

a soft start of the DC/DC apparatus, to thereby control the rise characteristics of the output voltage without depending on the load. Note that the explanation as to the "soft start" will be given later.

5 In the prior art, a design for the soft start control is made under the condition imagining the maximum load. Accordingly, where the load is light, the rise of the output voltage relatively becomes early, and thus it is difficult to finely control the rise of the output voltage
10 using only the soft start control.

Contrary to this, according to the present invention, it is possible to control the power turn-on sequence without depending on the load, only by changing circuit constants of the capacitor circuit for use in a soft start
15 of a DC/DC apparatus using a plurality of power supplies.

Also, when the power supply to each DC/DC apparatus is turned off, a difference is made between the times required until the respective output voltages reach 0V, depending on lightness or heaviness of the respective
20 loads and their load capacitances. In this case, if the power turn-off sequence is not properly controlled, the above latch-up phenomenon would be caused in semiconductor devices. Where such a latch-up is caused, some of the devices may be burned out.

25 According to the present invention, when the power supply to each DC/DC apparatus is turned off, a synchronous rectifying transistor or a load capacitance discharging transistor provided in each DC/DC apparatus is forcibly turned off to discharge charges corresponding to
30 the load capacitance. Thus, it is possible to remove the disadvantage in that a difference is made between the times required until the respective output voltages reach 0V.

BRIEF DESCRIPTION OF THE DRAWINGS

35 Other constitutional features and modes of operation of the present invention will be described hereinafter in detail by way of preferred embodiments with reference to

the accompanying drawings, in which:

Figs. 1a and 1b are diagrams showing the circuit constitution of a prior art DC/DC apparatus;

Fig. 2 is a waveform diagram representing an
5 operation of the DC/DC control circuit shown in Fig. 1b;

Figs. 3a and 3b are waveform diagrams of the input voltages of the PWM comparator shown in Fig. 1b;

Fig. 4 is an explanatory diagram of the rise characteristics of the output voltage of the prior art
10 DC/DC apparatus;

Fig. 5 is an explanatory diagram of the fall characteristics of the output voltage of the prior art DC/DC apparatus;

Fig. 6 is a diagram showing the circuit constitution
15 by which turn-on/turn-off sequences are controlled between the two power supplies using the prior art DC/DC apparatus;

Fig. 7 is an explanatory diagram of the rise/fall characteristics of the output voltages based on the
20 circuit constitution of Fig. 6;

Fig. 8 is a diagram showing the circuit constitution by which the two power supplies are simultaneously turned on using the prior art DC/DC apparatus;

Fig. 9 is an explanatory diagram of the rise characteristics of the output voltages based on the
25 circuit constitution of Fig. 8;

Fig. 10 is a diagram showing the fundamental constitution of the DC/DC apparatus according to a first aspect of the present invention;

Fig. 11 is a diagram showing the fundamental constitution of the DC/DC apparatus according to a second aspect of the present invention;

Figs. 12a and 12b are diagrams showing the circuit constitution of an embodiment of the DC/DC apparatus according to the first aspect of the present invention;
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Fig. 13 is a diagram showing a constitution of the error amplifier shown in Fig. 12b;

Fig. 14 is a waveform diagram representing an operation of the error amplifier of Fig. 13;

Fig. 15 is a waveform diagram representing an operation of the PWM comparator shown in Fig. 12b;

5 Fig. 16 is a diagram showing the circuit constitution by which a turn-on sequence is controlled between the two power supplies using the DC/DC apparatus according to the first aspect of the present invention;

10 Fig. 17 is an explanatory diagram of the rise characteristics of the output voltages based on the circuit constitution of Fig. 16;

15 Fig. 18 is a diagram showing the circuit constitution by which the two power supplies are simultaneously turned on using the DC/DC apparatus according to the first aspect of the present invention;

Fig. 19 is an explanatory diagram of the rise characteristics of the output voltages based on the circuit constitution of Fig. 18;

20 Figs. 20a and 20b are diagrams showing the circuit constitution of the DC/DC apparatus by which a power turn-off sequence is controlled based on the first aspect of the present invention;

25 Fig. 21 is an explanatory diagram of the fall characteristics of the output voltage based on the circuit constitution of Figs. 20a and 20b;

Figs. 22a and 22b are diagrams showing the circuit constitution of an embodiment of the DC/DC apparatus according to the second aspect of the present invention;

30 Fig. 23 is a diagram showing the circuit constitution by which turn-on/turn-off sequences are controlled between the two power supplies using the DC/DC apparatus according to the second aspect of the present invention;

35 Fig. 24 is an explanatory diagram of the rise/fall characteristics of the output voltages based on the circuit constitution of Fig. 23;

Fig. 25 is a diagram showing the circuit constitution by which the two power supplies are simultaneously turned

on/off using the DC/DC apparatus according to the second aspect of the present invention; and

Fig. 26 is an explanatory diagram of the rise/fall characteristics of the output voltages based on the circuit constitution of Fig. 25.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First, for better understanding of the preferred embodiments of the present invention, the related prior art will be explained with reference to Figs. 1a to 9.

Figure 1a shows the circuit constitution of a DC/DC apparatus used in an ordinary hand-held type personal computer or the like.

In Fig. 1a, reference ON denotes an on/off control signal for indicating a start (on) or a stop (off) of the operation of the DC/DC apparatus, and reference 30 denotes a DC/DC control circuit using a PWM control and responsive to the on/off control signal ON. Under control of the DC/DC control circuit 30, the DC/DC apparatus starts its operation when the on/off control signal ON is at "H" level, and stops its operation when the on/off control signal ON is at "L" level. Also, reference TR31 denotes a switching transistor which is turned on/off in response to an output DH of the DC/DC control circuit 30; reference L31 denotes a choke coil for converting an input voltage VI to an output voltage VO1; reference D31 denotes a fly-wheel diode for releasing energy accumulated in the choke coil L31 when the transistor TR31 is in off state; reference C31 denotes a capacitor for smoothing its input voltage (voltage at the output side of the choke coil L31); and reference C32 denotes a soft start capacitor for preventing rush current from flowing into the circuit when the operation of the DC/DC apparatus is started.

Note that, in the description below, "capacitor" indicates a soft start capacitor so long as a special definition is not given thereto.

Figure 1b shows the constitution of the DC/DC control

circuit 30 shown in Fig. 1a.

In Fig. 1b, references R31 and R32 each denote a resistor for dividing the output voltage VO1 of the DC/DC apparatus, and respective resistance values are selected so that the divided voltage obtained when the output voltage VO1 is at a rated value becomes the same as a reference voltage E31. Also, reference 31 denotes an error amplifier for amplifying a difference between the voltage divided by the resistors R31 and R32 and the reference voltage E31; reference 32 denotes a triangular wave oscillator for oscillating a triangular wave signal at a constant frequency; and reference 33 denotes a PWM comparator for controlling a width (i.e., on period) of its output pulse according to an output voltage of the error amplifier 31. The PWM comparator 33 compares a voltage of the triangular wave signal from the oscillator 32 with both the output voltage of the error amplifier 31 and a terminal voltage of the capacitor C32, and is brought to on state when the voltage of the triangular wave signal is lower than any one of the two voltages, to thereby bring a subsequent driver 34 to on state. As a result, the output DH of the driver 34 is made "H" level and thus the switching transistor TR31 is turned on. Also, reference 35 denotes a power supply unit which responds to the on/off control signal ON and controls on/off of the power supply to the DC/DC control circuit 30 to thereby control on/off (start/stop of the operation) of the entire DC/DC apparatus. Also, reference TR32 denotes a transistor for discharging charges of the capacitor C32 to set the terminal voltage thereof to 0 V when the operation of the DC/DC apparatus is stopped; and reference I31 denotes a constant current source for charging the capacitor C32 to raise the terminal voltage thereof in a constant time when the transistor TR32 is in off state.

Referring to Fig. 1a, the diode D31 forms a current path together with the choke coil L31 when the transistor

TR31 is in off state. The transistor TR31 is controlled by the frequency of the output DH of the DC/DC control circuit 30, so as to keep the output voltage VO1 at a constant value. When the transistor TR31 is in on state, the input voltage VI is supplied to the LC circuit (the choke coil L31 and the capacitor C31). When the transistor TR31 is turned off, the energy accumulated in the choke coil L31 is supplied via the diode D31 to the load. At this time, the smoothing capacitor C31 smoothes its input voltage to provide the output voltage VO1.

Assuming that one cycle period of the on/off operation of the transistor TR31 is T; the period during which the transistor TR31 is in on state is Ton; and the period during which the transistor TR31 is in off state is Toff, the output voltage VO1 is expressed by the following equation.

$$VO1 = [Ton / (Ton + Toff)] \times VI = (Ton / T) \times VI$$

Also, the current to flow through the choke coil L31 is fed from the input end (VI) when the transistor TR31 is in on state, and is fed via the diode D31 when the transistor TR31 is in off state. Accordingly, an average input current (Iin) is equal to the product of a duty (Ton/T) of the transistor TR31 and an output current (Iout), and thus is expressed by the following equation.

$$Iin = (Ton / T) \times Iout$$

From this equation, it will be appreciated that it is possible to compensate a fluctuation of the input voltage by controlling the duty cycle. In the same way, where the output voltage VO1 fluctuates depending on a fluctuation of the load, it is possible to keep the output voltage VO1 at a constant value by detecting the voltage VO1 and controlling the duty cycle.

Figure 2 shows waveforms representing an operation of the DC/DC control circuit 30.

First, for simplification of the explanation, the operation as to the case where the capacitor C32 is not provided will be explained.

The output voltage VO1 is suitably divided by the resistors R31 and R32 and the divided voltage is input to the error amplifier 31. The error amplifier 31 amplifies a difference between the divided voltage and the reference voltage E31, and outputs the amplified voltage to the PWM comparator 33. As described above, the PWM comparator 33 controls the width of its output pulse based on a comparison of the output voltage of the error amplifier 31 with the triangular wave voltage. Accordingly, when the output voltage of the error amplifier 31 becomes larger, the output pulse width of the PWM comparator 33 accordingly becomes wider. On the other hand, when the output voltage of the error amplifier 31 becomes smaller, the output pulse width of the PWM comparator 33 accordingly becomes narrower. Therefore, when the output voltage VO1 is lowered, the output voltage of the error amplifier 31 becomes large and thus the output pulse width of the PWM comparator 33 becomes wide. As a result, the on period (Ton) of the transistor TR31 becomes long. Inversely, when the output voltage VO1 is heightened, the output voltage of the error amplifier 31 becomes small and thus the output pulse width of the PWM comparator 33 becomes narrow. As a result, the on period (Ton) of the transistor TR31 becomes short.

Thus, in the DC/DC apparatus using a PWM control, it is possible to control the output voltage VO1 by controlling the on/off ratio of the switching transistor TR31.

By the way, since the output voltage VO1 is 0V when the operation of the DC/DC apparatus is started, the difference between the input voltage VI and the output voltage VO1 is the maximum and thus the output voltage of the error amplifier 31 is also the maximum. Accordingly, the output pulse width of the PWM comparator 33 becomes the maximum and thus the on period (Ton) of the transistor TR31 also becomes the maximum. Also, the

maximum current (I_{peak}) flowing through the choke coil L31 is determined by an inductance (L) of the choke coil L31, the input voltage V_I , the output voltage V_{O1} and the on period (T_{on}) of the transistor TR31, and is expressed by the following equation:

$$I_{peak} = [(V_I - V_{O1})/L] \times T_{on}$$

From this equation, it will be appreciated that an excessive rush current flows through the transistor TR31 and the choke coil L31 since the output voltage V_{O1} is 0V and the on period (T_{on}) of the transistor TR31 is the maximum when the operation of the DC/DC apparatus is started.

To solve such a drawback, a control of temporarily reducing the on period (T_{on}) when the operation of the DC/DC apparatus is started is carried out. Such a control is called "soft start".

Referring back to Fig. 1b, the capacitor C32 is provided to carry out the soft start. By the operation of the capacitor C32, it is possible to lower one of a plurality of non-inverting input voltages input to the PWM comparator 33 when the operation of the DC/DC apparatus is started, and thus to forcibly reduce the on period (T_{on}). As a result, it is possible to prevent an excessive rush current from flowing into the circuit.

The PWM comparator 33 compares the output voltage of the triangular wave oscillator 32 with both the output voltage of the error amplifier 31 and the voltage of the capacitor C32, and is brought to on state only when the triangular wave voltage is lower than any one of the two voltages, to thereby control the driver 34 to turn on the transistor TR31. When the operation of the DC/DC apparatus is started, the output voltage of the error amplifier 31 is the maximum, but the voltage of the capacitor C32 is around 0V. Accordingly, the output pulse width of the PWM comparator 33 is mainly controlled by the voltage of the capacitor C32, and is not substantially controlled by the output voltage of the

error amplifier 31. As a result, the output pulse width of the PWM comparator 33 becomes extremely short.

As is appreciated from the above equation, even if the output voltage VO1 is extremely small, it is possible to limit the quantity of the rush current flowing into the choke coil L31 by reducing the on period (T_{on}) of the transistor TR31. Since the voltage of the capacitor C32 is charged by the constant current source I31, the output pulse width of the PWM comparator 33 gradually becomes long according to the rise of the voltage of the capacitor C32. As a result, the output voltage VO1 also gradually rises and thus the current flowing into the choke coil L31 is not excessively increased. When the voltage of the capacitor C32 then exceeds the output voltage of the error amplifier 31, the DC/DC apparatus is controlled with a pulse width determined by the output voltage of the error amplifier 31.

Thus, by making the on period (T_{on}) gradually long according to the charging time constant of the capacitor C32, it is possible to suppress the rush current.

Next, the relationship between the rise characteristics of the output voltage obtained when the power supply to the DC/DC apparatus is turned on and the load will be explained.

As described above, the on period (T_{on}) of the transistor TR31 is determined by a voltage of a lower potential among the two non-inverting input voltages (i.e., the output voltage of the error amplifier 31 and the voltage of the capacitor C32) input to the PWM comparator 33.

Figures 3a and 3b show waveforms of the input voltages of the PWM comparator 33 in the case where the load is light, and in the case where the load is heavy, respectively.

At a point of time t_0 when the power supply to the DC/DC apparatus is turned on, the output voltage of the error amplifier 31 is the maximum, but the voltage of the

capacitor C32 is around 0V. Accordingly, the on period (T_{on}) of the transistor TR31 is determined only by the voltage of the capacitor C32.

5 With a lapse of time, the voltage of the capacitor C32 gradually rises with a gradient determined by the capacitance of the capacitor C32. On the other hand, the output voltage of the error amplifier 31 gradually falls since the output voltage VO1 gradually rises. Then, after a lapse of time (a point of time t_1 in Fig. 3a, and
10 a point of time t_2 in Fig. 3b), the voltage of the capacitor C32 exceeds the output voltage of the error amplifier 31. Thereafter, the on period (T_{on}) of the transistor TR31 is controlled by the output voltage of the error amplifier 31.

15 From the above, at a point of time before the cross point at which the voltage curve of the capacitor C32 intersects the output voltage curve of the error amplifier 31, the on period (T_{on}) of the transistor TR31 is controlled only by the voltage of the capacitor C32, regardless of the output voltage VO1. At this time, the
20 current to be fed to the output side of the DC/DC apparatus substantially becomes constant.

Accordingly, where the load of the DC/DC apparatus is light (see Fig. 3a), the output voltage VO1 begins to
25 rise in a relatively short time (at the point of time t_1), and where the load of the DC/DC apparatus is heavy (see Fig. 3b), the output voltage VO1 begins to rise at the point of time t_2 later than the point of time t_1 . As described above, the output voltage of the error
30 amplifier 31 is obtained by amplifying the difference between the reference voltage E31 and the divided voltage proportional to the output voltage VO1. Accordingly, at a point of time t_x before the cross point, the lighter the load of the DC/DC apparatus becomes, the lower the output
35 voltage of the error amplifier 31 becomes, and the heavier the load of the DC/DC apparatus becomes, the higher the output voltage of the error amplifier 31 becomes.

Namely, the lighter the load of the DC/DC apparatus becomes, the shorter the time necessary to reach the cross point becomes, and the heavier the load of the DC/DC apparatus becomes, the longer the time necessary to reach the cross point becomes. This means that the rise characteristics of the output voltage of the DC/DC apparatus differ depending on lightness or heaviness of the load, i.e., that the lighter the load becomes, the earlier the rise becomes, and the heavier the load becomes, the later the rise becomes.

The above will be explained with reference to Fig. 4.

When the on/off control signal ON is made "H" level at a point of time T_0 , the power supply to the DC/DC apparatus is turned on. Assuming that the load of the DC/DC apparatus is light, the output voltage of the DC/DC apparatus gradually rises and reaches the rated voltage VO_1 at a point of time T_1 . On the other hand, assuming that the load of the DC/DC apparatus is heavy, the output voltage of the DC/DC apparatus gradually rises, but cannot reach the rated voltage VO_1 at the point of time T_1 because of the heaviness of the load. Thereafter, the output voltage reaches the rated voltage VO_1 at a point of time T_2 .

Next, the fall characteristics of the output voltage obtained when the power supply to the DC/DC apparatus is turned off will be explained with reference to Fig. 5.

The fall of the output voltage is determined by the time required for discharging charges accumulated in the smoothing capacitor C31 which is the load capacitance of the DC/DC apparatus. When the on/off control signal ON is changed from "H" level to "L" level at a point of time T_0 , the power supply to the DC/DC apparatus is turned off. Assuming that the load of the DC/DC apparatus is heavy, the output voltage of the DC/DC apparatus gradually falls and reaches 0V at a point of time T_1 . On the other hand, assuming that the load of the DC/DC apparatus is

light, the output voltage of the DC/DC apparatus gradually falls, but cannot reach 0V at the point of time T1 because of the lightness of the load. Thereafter, the output voltage reaches 0V at a point of time T2.

5 As explained above, according to the prior art, where the load of the DC/DC apparatus is heavy, the output voltage of the DC/DC apparatus rises in proportion to the quantity of charges accumulated in the capacitor C32. Accordingly, the output voltage exhibits the rise
10 characteristics depending on a time constant determined by the capacitance of the capacitor C32. Contrary to this, where the load of the DC/DC apparatus is light, the output voltage of the DC/DC apparatus rises in a shorter time than the time constant determined by the capacitance
15 of the capacitor C32.

Thus, the prior art capacitor circuit provided to carry out the soft start has only the function of preventing an excessive rush current from flowing into the DC/DC apparatus, and does not have a function of
20 controlling the rise characteristics of the output voltage of the DC/DC apparatus.

Also, where a plurality of power supplies are used in an electronic apparatus, if turn-on/turn-off sequences between the respective power supplies are not fully taken
25 into consideration, a latch-up phenomenon may be caused in semiconductor devices used in the electronic apparatus and thus some devices may be burned out. As described above, the rise characteristics of the output voltage obtained when the power supply to the DC/DC apparatus is
30 turned on depend on the load of the DC/DC apparatus, and thus it is substantially impossible to control the rise characteristics using only the soft start capacitor. Therefore, to control the turn-on sequence between the plurality of power supplies, a special logic circuit for
35 the sequence control is required.

Figure 6 shows the circuit constitution by which turn-on/turn-off sequences are controlled between the two

power supplies (the DC/DC apparatuses DC10 and DC20), and Fig. 7 shows the rise/fall characteristics of the output voltages based on the circuit constitution.

The constitution of each of the DC/DC apparatuses DC10 and DC20 is the same as that of the DC/DC apparatus shown in Fig. 1a, and thus the explanation thereof is omitted. Accordingly, only the explanation as to the circuit portion which controls power turn-on/turn-off sequences with respect to the DC/DC apparatuses DC10 and DC20 is given.

In Fig. 6, reference IC311 denotes a voltage comparator for comparing an output voltage VO1 of the DC/DC apparatus DC10 with a reference voltage E311. The voltage comparator IC311 outputs a "H" level signal when the output voltage VO1 is equal to or above the reference voltage E311, and outputs a "L" level signal when the output voltage VO1 is below the reference voltage E311. Reference IC312 denotes a voltage comparator for comparing an output voltage VO2 of the DC/DC apparatus DC20 with a reference voltage E312. The voltage comparator IC312 outputs a "H" level signal when the output voltage VO2 is equal to or above the reference voltage E312, and outputs a "L" level signal when the output voltage VO2 is below the reference voltage E312. Also, reference OR11 denotes an OR gate responsive to the on/off control signal ON and an output signal of the voltage comparator IC312, and reference AD12 denotes an AND gate responsive to the on/off control signal ON and an output signal of the voltage comparator IC311. When the OR gate OR11 outputs a "H" level signal, the DC/DC control circuit 301 is enabled to start the operation of the DC/DC apparatus DC10. In the same way, when the AND gate AD12 outputs a "H" level signal, the DC/DC control circuit 302 is enabled to start the operation of the DC/DC apparatus DC20.

When the on/off control signal ON is at "L" level, the respective operations of the DC/DC apparatuses DC10

and DC20 are stopped, and thus the voltage comparators IC311 and IC312 output a "L" level signal, respectively.

When the on/off control signal ON is made "H" level and thus the power turn-on of the DC/DC apparatuses DC10 and DC20 is instructed, the OR gate OR11 outputs a "H" level signal to the DC/DC control circuit 301 and thus the operation of the DC/DC apparatus DC10 is started. On the other hand, the AND gate AD12 continues to output a "L" level signal to the DC/DC control circuit 302 since the output signal of the voltage comparator IC311 is still at "L" level. Accordingly, the operation of the DC/DC apparatus DC20 is still stopped. As a result, only the power supply to the DC/DC apparatus DC10 is turned on.

When the power turn-on sequence of the DC/DC apparatus DC10 is completed and the output voltage VO1 exceeds the reference voltage E311, the output signal of the voltage comparator IC311 is changed to "H" level. As a result, the AND gate AD12 outputs a "H" level signal and thus the operation of the DC/DC apparatus DC20 is started.

Also, when the power turn-on sequence of the DC/DC apparatus DC20 is completed and the output voltage VO2 exceeds the reference voltage E312, the output signal of the voltage comparator IC312 is changed to "H" level. Since the OR gate OR11 outputs a "H" level signal when at least one of the on/off control signal ON and the output signal of the voltage comparator IC312 is at "H" level, the OR gate OR11 continues to output the "H" level signal to the DC/DC control circuit 301. Accordingly, as long as the on/off control signal ON is thereafter at "H" level, the DC/DC apparatuses DC10 and DC20 continue the respective operations, and thus the voltage comparators IC311 and IC312 continue to output a "H" level signal, respectively.

Next, when the on/off control signal ON is made "L" level and thus the power turn-off of the DC/DC apparatuses DC10 and DC20 is instructed, the AND gate AD12

outputs a "L" level signal to the DC/DC control circuit 302 and thus the operation of the DC/DC apparatus DC20 is stopped. On the other hand, the OR gate OR11 continues to output a "H" level signal to the DC/DC control circuit 301 since the output signal of the voltage comparator IC312 is still at "H" level. Accordingly, the operation of the DC/DC apparatus DC10 is still maintained. As a result, only the power supply to the DC/DC apparatus DC20 is turned off.

10 When the power turn-off sequence of the DC/DC apparatus DC20 is completed and the output voltage VO2 is below the reference voltage E312, the output signal of the voltage comparator IC312 is changed to "L" level. As a result, the OR gate OR11 outputs a "L" level signal and thus the operation of the DC/DC apparatus DC10 is stopped.

15 Also, when the power turn-off sequence of the DC/DC apparatus DC10 is completed and the output voltage VO1 is below the reference voltage E311, the output signal of the voltage comparator IC311 is changed to "L" level. Since the AND gate AD12 outputs a "L" level signal when at least one of the on/off control signal ON and the output signal of the voltage comparator IC311 is at "L" level, the AND gate AD12 continues to output the "L" level signal to the DC/DC control circuit 302. Accordingly, as long as the on/off control signal ON is thereafter at "L" level, the respective operations of the DC/DC apparatuses DC10 and DC20 continue to be stopped, and thus the voltage comparators IC311 and IC312 continue to output a "L" level signal, respectively.

20 The above will be explained with reference to Fig. 7.

25 When the on/off control signal ON is made "H" level at a point of time T0, the power supply to the DC/DC apparatus DC10 is turned on. Accordingly, the output voltage of the DC/DC apparatus DC10 gradually rises and reaches the rated voltage VO1 at a point of time T1. At this time, the power supply to the DC/DC apparatus DC20

is not yet turned on. When the output voltage of the DC/DC apparatus DC10 reaches the rated voltage VO1 at the point of time T1, the AND gate AD12 outputs a "H" level signal and thus the power supply to the DC/DC apparatus DC20 is turned on. As a result, the output voltage of the DC/DC apparatus DC20 gradually rises and reaches the rated voltage VO2 at a point of time T2. Thus, the power turn-on sequences of the DC/DC apparatuses DC10 and DC20 are controlled.

Next, when the on/off control signal ON is made "L" level at a point of time T3, the AND gate AD12 outputs a "L" level signal and thus the power turn-off of the DC/DC apparatus DC20 is instructed. Accordingly, the output voltage of the DC/DC apparatus DC20 gradually falls and reaches 0V at a point of time T4. At this time, the power supply to the DC/DC apparatus DC10 is not yet turned off. When the output voltage of the DC/DC apparatus DC20 reaches 0V at the point of time T4, the OR gate OR11 outputs a "L" level signal and thus the power supply to the DC/DC apparatus DC10 is turned off. As a result, the output voltage of the DC/DC apparatus DC10 gradually falls and reaches 0V at a point of time T5. Thus, the power turn-off sequences of the DC/DC apparatuses DC10 and DC20 are controlled.

As explained above, where the power turn-on/turn-off sequences are controlled between the two DC/DC apparatuses, the logic circuit (OR gate OR11, AND gate AD12, voltage comparators IC311 and IC312, and the like) for the sequence control must be provided in addition to the DC/DC apparatuses. Namely, it is substantially impossible to control the power turn-on/turn-off sequences using only the DC/DC apparatuses.

Figure 8 shows the circuit constitution by which the two power supplies (the DC/DC apparatuses DC30 and DC40) are simultaneously turned on, and Fig. 9 shows the rise characteristics of the output voltages based on the circuit constitution.

The constitution of each of the DC/DC apparatuses DC30 and DC40 is the same as that of the DC/DC apparatus shown in Fig. 1a, and thus the explanation thereof is omitted.

5 In the constitution of Fig. 8, the on/off control signal ON is commonly input to the DC/DC apparatuses DC30 and DC40 so as to simultaneously turn on the respective power supplies thereof. When the on/off control signal ON is at "L" level, the respective operations of the
10 DC/DC apparatuses DC30 and DC40 are stopped.

 When the on/off control signal ON is made "H" level, the respective power turn-on sequences of the DC/DC apparatuses DC30 and DC40 are started. However, as explained with reference to Figs. 1a to 3b, the respective
15 rise characteristics of the output voltage VO3 of the DC/DC apparatus DC30 and the output voltage VO4 of the DC/DC apparatus DC40 depend on lightness or heaviness of the respective loads. Accordingly, it cannot be ensured that the output voltages VO3 and VO4 rise simultaneously.

20 The above will be explained with reference to Fig. 9.

 When the on/off control signal ON is made "H" level at a point of time T0, the power supplies to the DC/DC apparatuses DC30 and DC40 are turned on. Assuming that
25 the load of the DC/DC apparatus DC30 is heavier than that of the DC/DC apparatus DC40, the output voltage of the DC/DC apparatus DC40 gradually rises and reaches the rated voltage VO4 at a point of time T1. On the other hand, the output voltage of the DC/DC apparatus DC30
30 gradually rises, but cannot reach the rated voltage VO3 at the point of time T1 because of the heaviness of the load. Thereafter, the output voltage of the DC/DC apparatus DC30 reaches the rated voltage VO3 at a point of time T2.

35 Thus, in the prior art, where the power supplies are simultaneously turned on with respect to the two DC/DC apparatuses, it is substantially impossible to control

the rise characteristics of the respective output voltages since the rise characteristics depend on lightness or heaviness of the respective loads. As a result, in a system using a plurality of power supplies, a drawback occurs in that a latch-up phenomenon is caused in semiconductor devices and thus some devices are burned out.

Figure 10 shows the fundamental constitution of the DC/DC apparatus according to the first aspect of the present invention.

In Fig. 10, reference 10 denotes a DC/DC control circuit using a PWM control; reference 11 denotes an error amplifier for voltage control; reference 12 denotes a triangular wave oscillator for oscillating (and generating) a triangular wave signal; reference 13 denotes a PWM comparator for comparing an output voltage of the error amplifier 11 with an output voltage of the triangular wave oscillator 12 and controlling an on period of its output pulse; reference 14 denotes a driver for driving a switching transistor (not shown in Fig. 10); reference 15 denotes a soft start capacitor; references 16 and 17 denote corresponding reference voltage circuits supplying respective reference voltages to the error amplifier 11; reference 18 denotes a load capacitance discharging circuit for forcibly discharging charges corresponding to the load capacitance when the operation of the DC/DC apparatus is stopped; and reference DCG denotes a discharging control signal indicating validity or invalidity of the discharging with respect to the load capacitance discharging circuit 18.

In a preferred aspect of the present invention, the error amplifier 11 includes a first input terminal 111 for inputting a voltage signal obtained from an output voltage of a DC/DC result, a second input terminal 112 for inputting a predetermined reference voltage signal, a third input terminal 113 for inputting a reference voltage signal used as a soft start signal when a power supply to the DC/DC apparatus is turned on. The error amplifier 11

amplifies a difference between a voltage signal input from the first input terminal 111 and a voltage signal of a lower potential, among the voltage signals input from the second and third input terminals 112 and 113. Based on an output of the error amplifier 11, the PWM comparator 13 carries out the pulse width modulation control. Accordingly, it is possible to control the rise characteristics of the output voltage obtained when the power supply to the DC/DC apparatus is turned on, without depending on lightness or heaviness of the load.

Also, the capacitor 15 is provided for supplying the reference voltage via the reference voltage circuit 16 to the third input terminal 113 of the error amplifier 11, and the reference voltage is continuously changed between 0V and the rated voltage. Accordingly, it is possible to prevent overshoots from occurring in the output voltage.

Also, in another preferred aspect of the present invention, a plurality of DC/DC control circuits, each being the DC/DC control circuit 10, are provided and a plurality of capacitors, each being the capacitor 15, are provided to correspond to the plurality of DC/DC control circuits on one-to-one basis, and respective capacitance values are properly changed between the plurality of capacitors. Accordingly, it is possible to easily control a turn-on sequence between the plurality of power supplies without using any special logic circuit for controlling the power turn-on sequence.

Also, in still another preferred aspect of the present invention, a plurality of DC/DC control circuits, each being the DC/DC control circuit 10, are provided and the capacitor 15 is provided to be shared by the plurality of DC/DC control circuits, and based on a time constant determined by a capacitance value of the capacitor 15, rise times of respective output voltages of DC/DC results controlled by the plurality of DC/DC control circuits are controlled. Accordingly, it is possible to control the rises of the respective output voltages so as to be the

same as each other.

Furthermore, in another preferred aspect of the present invention, the load capacitance discharging circuit 18 is provided for discharging charges
5 corresponding to the output voltage of a DC/DC result to be input to the error amplifier 11 when a power supply to the DC/DC apparatus is turned off. Accordingly, where a plurality of power supplies (i.e., DC/DC apparatuses) are used, it is possible to control the fall times of
10 respective output voltages so as to be the same as each other.

Also, the DC/DC control circuit 10 further includes means for inputting the discharging control signal DCG, and the load capacitance discharging circuit 18 is
15 operated when the validity of the discharging is indicated by the discharging control signal DCG. Accordingly, it is possible to control the discharging of the charges corresponding to the load capacitance by the external signal (discharging control signal DCG).

20 Figure 11 shows the fundamental constitution of the DC/DC apparatus according to the second aspect of the present invention.

In Fig. 11, reference 20 denotes a DC/DC control circuit using a synchronous rectifying control; reference
25 21 denotes an error amplifier for voltage control; reference 22 denotes a triangular wave oscillator for oscillating a triangular wave signal; reference 23 denotes a PWM comparator for comparing an output voltage of the error amplifier 21 with an output voltage of the
30 triangular wave oscillator 22 and controlling an on period of its output pulse; reference 24 denotes a driver for driving a switching transistor TR21; reference 25 denotes a synchronous rectifying control circuit; reference 26 denotes a driver for driving a synchronous
35 rectifying transistor TR22; reference 27 denotes a load capacitance discharging control circuit for controlling the discharging of charges corresponding to the load

capacitance when the operation of the DC/DC apparatus is stopped; and reference DCG denotes a discharging control signal indicating validity or invalidity of the discharging with respect to the load capacitance
5 discharging control circuit 27.

In a preferred aspect of the present invention, the load capacitance discharging control circuit 27 is provided for turning on the synchronous rectifying transistor TR22 to discharge charges corresponding to the
10 output voltage VO of a DC/DC result when a power supply to the DC/DC apparatus is turned off. Accordingly, where a plurality of DC/DC apparatuses using a synchronous rectifying control are used, it is possible to control the fall times of respective output voltages so as to be the
15 same as each other.

Also, the DC/DC control circuit 20 further includes means for inputting the discharging control signal DCG, and the load capacitance discharging control circuit 27 is operated when the validity of the discharging is
20 indicated by the discharging control signal DCG. Accordingly, it is possible to control the discharging of the charges corresponding to the load capacitance by the external signal (discharging control signal DCG).

Next, the preferred embodiments of the present
25 invention will be explained in detail with reference to Figs. 12a to 26.

Figures 12a and 12b show the circuit constitution of an embodiment (DC/DC apparatus using a PWM control) of the DC/DC apparatus according to the first aspect of the
30 present invention.

The constitution of the entire DC/DC apparatus shown in Fig. 12a is the same as that of the DC/DC apparatus shown in Fig. 1a, and thus the explanation thereof is omitted. Accordingly, only the explanation as to the
35 DC/DC control circuit 100 shown in Fig. 12b is given.

In Fig. 12b, references R1 and R2 each denote a resistor for dividing the output voltage VO1 of the DC/DC

apparatus; reference 11 denotes an error amplifier for amplifying a difference between the voltage divided by the resistors R1 and R2 and one of a plurality of reference voltages (in the illustrated example, a voltage of the capacitor C12 and a reference voltage E1); reference 12 denotes a triangular wave oscillator for oscillating a triangular wave signal at a constant frequency; and reference 13 denotes a PWM comparator for controlling an on period of its output pulse according to an output voltage of the error amplifier 11. The PWM comparator 13 compares a voltage of the triangular wave signal from the oscillator 12 with the output voltage of the error amplifier 11, and is brought to on state when the voltage of the triangular wave signal is lower than the output voltage of the error amplifier 11, to thereby bring a subsequent driver 14 to on state. As a result, the output DH of the driver 14 is made "H" level and thus the switching transistor TR11 is turned on. Also, reference 19 denotes a power supply unit which responds to the on/off control signal ON and controls on/off of the power supply to the DC/DC control circuit 100 to thereby control on/off (start/stop of the operation) of the entire DC/DC apparatus. Also, reference TR12 denotes a transistor for discharging charges of the capacitor C12 to set the terminal voltage thereof to 0V when the operation of the DC/DC apparatus is stopped; and reference I1 denotes a constant current source for charging the capacitor C12 to raise the terminal voltage thereof in a constant time when the transistor TR12 is in off state.

The constitution of the DC/DC control circuit 100 is substantially the same as that of the DC/DC control circuit 30 shown in Fig. 1b. The difference is that in the constitution of Fig. 1b, the capacitor C32 is connected to the non-inverting input of the PWM comparator 33; while in the constitution of the present embodiment (Fig. 12b), the capacitor C12 is connected to the non-inverting input of the error amplifier 11.

In Fig. 12b, the error amplifier 11 amplifies a difference between the voltage divided by the resistors R1 and R2 and a voltage of a lower potential among the reference voltage E1 and the voltage of the capacitor C12, and outputs the amplified voltage to the PWM comparator 13.

When the on/off control signal ON is at "L" level, the power supply unit 19 brings the entire DC/DC control circuit 100 to off state and turns on the transistor TR12 to thereby cause the terminal voltage of the capacitor C12 to be 0V.

When the on/off control signal ON is made "H" level and thus the power turn-on of the DC/DC apparatus is instructed, the DC/DC control circuit 100 starts its operation and the transistor TR12 is turned off. Accordingly, the charging to the capacitor C12 is started by the constant current source I1 and thus the voltage of the capacitor C12 gradually rises. After a lapse of time corresponding to the time constant determined by the capacitance of the capacitor C12 and the charging current value of the constant current source I1, the voltage of the capacitor C12 reaches the same voltage as the reference voltage E1.

The error amplifier 11 amplifies a difference between the inverting input voltage from the first input terminal 111 and a voltage of a lower potential among the non-inverting input voltages from the second and third input terminals 112 and 113, and outputs the amplified voltage to the PWM comparator 13. Accordingly, when the voltage of the capacitor C12 is lower than the reference voltage E1, the error amplifier 11 amplifies a difference between the divided voltage of the output voltage VO1 and the voltage of the capacitor C12, and when the voltage of the capacitor C12 is higher than the reference voltage E1, the error amplifier 11 amplifies a difference between the divided voltage of the output voltage VO1 and the reference voltage E1.

Figure 13 shows a constitution of the error amplifier 11.

As illustrated, the error amplifier 11 includes a comparator 114 for comparing voltages A and B input from the second and third input terminals 112 and 113 and outputting a voltage of a lower potential as its output voltage Q; and a differential amplifier 115 for amplifying a difference between the output voltage Q of the comparator 114 and a voltage R input from the first input terminal 111 and outputting the amplified voltage as its output voltage Z.

According to the present embodiment, since the control is carried out so as to gradually raise the reference voltage which determines the output voltage of the DC/DC apparatus, and to provide the rated output voltage VO1 after a constant time, the output voltage of the DC/DC apparatus can be controlled by the time constant determined by the capacitance of the capacitor C12, without depending on the load of the DC/DC apparatus. Namely, the smaller the capacitance of the capacitor C12 becomes, the shorter the rise time of the output voltage of the DC/DC apparatus becomes, and the larger the capacitance of the capacitor C12 becomes, the longer the rise time of the output voltage of the DC/DC apparatus becomes. Accordingly, by suitably selecting the capacitance of the capacitor C12, it is possible to arbitrarily control the rise characteristics of the output voltage of the DC/DC apparatus.

The above will be explained with reference to Fig. 14.

When the on/off control signal ON is made "H" level at a point of time T0, the operation of the DC/DC apparatus is started. Accordingly, the voltage of the capacitor C12 gradually rises and reaches the same voltage as the reference voltage E1 at a point of time T1. The output voltage of the DC/DC apparatus also gradually rises and reaches the rated voltage VO1 at the point of

time T1. Namely, in the period from the point of time T0 to the point of time T1, the error amplifier 11 amplifies a difference between the divided voltage of the output voltage VO1 and the voltage of the capacitor C12, and
5 after the point of time T1, the error amplifier 11 amplifies a difference between the divided voltage and the reference voltage E1.

Figure 15 shows waveforms representing an operation of the PWM comparator 13.

10 As illustrated, the PWM comparator 13 outputs a "H" level signal when the output voltage of the error amplifier 11 is higher than the output voltage of the triangular wave oscillator 12, and outputs a "L" level signal when the output voltage of the error amplifier 11
15 is lower than the triangular wave voltage. As described above, the error amplifier 11 uses the voltage of the capacitor C12 as its reference voltage until the output voltage of the DC/DC apparatus reaches the rated voltage VO1. Accordingly, the output voltage of the DC/DC
20 apparatus exhibits 0V at the point of time T0 and exhibits the rated voltage VO1 at the point of time T1, without depending on lightness or heaviness of the load thereof.

Figure 16 shows the circuit constitution by which a turn-on sequence is controlled between the two power
25 supplies (the DC/DC apparatuses DC1 and DC2), and Fig. 17 shows the rise characteristics of the output voltages based on the circuit constitution.

In Fig. 16, the constitution of each of the DC/DC apparatuses DC1 and DC2 is the same as that of the DC/DC
30 apparatus shown in Fig. 12a. As described above, the respective rise characteristics of the output voltages VO1 and VO2 of the DC/DC apparatuses DC1 and DC2 are determined by the respective capacitances of the capacitors C121 and C122 without depending on lightness
35 or heaviness of the corresponding loads.

Accordingly, for example, where the power supply to the DC/DC apparatus DC1 is first turned on and the power

supply to the DC/DC apparatus DC2 is then turned on, such a power turn-on sequence can be realized by setting the capacitance of the capacitor C121 to be smaller than that of the capacitor C122.

5 The above will be explained with reference to Fig. 17.

 The on/off control signal ON is commonly input to the DC/DC apparatuses DC1 and DC2 so as to simultaneously turn on the respective power supplies thereof. The capacitance of the capacitor C121 is selected so that the
10 output voltage of the DC/DC apparatus DC1 reaches the rated voltage VO1 at a point of time T1, and the capacitance of the capacitor C122 is selected so that the output voltage of the DC/DC apparatus DC2 reaches the rated voltage VO2 at a point of time T2.

15 When the on/off control signal ON is at "L" level, the respective operations of the DC/DC apparatuses DC1 and DC2 are stopped. When the on/off control signal ON is made "H" level at the point of time T0, the respective power turn-on sequences of the DC/DC apparatuses DC1 and
20 DC2 are simultaneously started. Accordingly, the output voltage of the DC/DC apparatus DC1 reaches the rated voltage VO1 at the point of time T1, depending on the capacitance of the capacitor C121, and the output voltage of the DC/DC apparatus DC2 reaches the rated voltage VO2
25 at the point of time T2, depending on the capacitance of the capacitor C122.

 Thus, it is possible to control the respective rise characteristics of the output voltages of the DC/DC apparatuses DC1 and DC2 using only the capacitors C121
30 and C122.

 Figure 18 shows the circuit constitution by which the two power supplies (the DC/DC apparatuses DC3 and DC4) are simultaneously turned on, and Fig. 19 shows the rise characteristics of the output voltages based on the
35 circuit constitution.

 In Fig. 18, the on/off control signal ON is commonly input to the DC/DC apparatuses DC3 and DC4 so as to

simultaneously turn on the respective power supplies thereof.

When the on/off control signal ON is at "L" level, the respective operations of the DC/DC apparatuses DC3 and DC4 are stopped. When the on/off control signal ON is made "H" level, the respective power turn-on sequences of the DC/DC apparatuses DC3 and DC4 are simultaneously started. At this time, since the capacitor C123 is commonly connected to the DC/DC apparatuses DC3 and DC4, the reference voltage (i.e., voltage of the capacitor C123) of the DC/DC apparatus DC3 and the reference voltage (i.e., voltage of the capacitor C123) of the DC/DC apparatus DC4 begin to rise simultaneously and, after a lapse of certain time, reach the same voltage as the reference voltage E1 simultaneously. Accordingly, the time required until the output voltage of the DC/DC apparatus DC3 reaches the rated voltage V03 is equal to the time required until the output voltage of the DC/DC apparatus DC4 reaches the rated voltage V04.

The above will be explained with reference to Fig. 19.

When the on/off control signal ON is made "H" level at a point of time T0, the respective operations of the DC/DC apparatuses DC3 and DC4 are started. Accordingly, the voltage of the capacitor C123 gradually rises and reaches the same voltage as the reference voltage E1 at a point of time T1. The output voltage of the DC/DC apparatus DC3 also gradually rises and reaches the rated voltage V03 at the point of time T1, and the output voltage of the DC/DC apparatus DC4 also gradually rises and reaches the rated voltage V04 at the point of time T1.

As explained above, where a turn-on sequence between a plurality of power supplies (DC/DC apparatuses) must be taken into consideration, such a power turn-on sequence can be easily controlled by setting the capacitance of the capacitor of a DC/DC apparatus to which the power supply is first turned on, to be smaller than that of the capacitor of a DC/DC apparatus to which the power supply

is next turned on. Accordingly, it becomes unnecessary to provide a special logic circuit for the power turn-on sequence control as required in the prior art.

Also, by providing the capacitor C123 commonly to the two DC/DC apparatuses as shown in Fig. 18, it is possible to realize the same rise characteristics with respect to the respective DC/DC apparatuses, without depending on lightness or heaviness of the respective loads.

Figures 20a and 20b show the circuit constitution of the DC/DC apparatus by which a power turn-off sequence is controlled based on the first aspect of the present invention, and Fig. 21 shows the fall characteristics of the output voltage based on the circuit constitution.

The constitution of the DC/DC apparatus shown in Fig. 20a is the same as that of the DC/DC apparatus shown in Fig. 12a, except that a discharging control signal DCG indicating validity or invalidity of the discharging of charges corresponding to the load capacitance is input to a DC/DC control circuit 105. As shown in Fig. 20b, the DC/DC control circuit 105 includes a load capacitance discharging circuit 18. In Fig. 20b, circuit portions other than the load capacitance discharging circuit 18 are the same as the corresponding portions of the DC/DC control circuit 100 shown in Fig. 12b, and thus the explanation thereof is omitted.

In Fig. 20b, reference IV1 denotes an inverter responsive to the on/off control signal ON; reference AD1 denotes an AND gate responsive to an output of the inverter IV1 and the discharging control signal DCG; and reference TR13 denotes a transistor responsive to an output of the AND gate AD1. When the output of the AND gate AD1 is at "H" level, the transistor TR13 is turned on to short-circuit the output end (VO1) of the DC/DC apparatus to the ground to thereby forcibly discharge charges corresponding to the load capacitance.

When the on/off control signal ON is at "H" level, or when the discharging control signal DCG is at "L" level,

the AND gate AD1 outputs a "L" level signal and thus the transistor TR13 is turned off. Accordingly, in this case, the operation of the DC/DC control circuit 105 is the same as the operation obtained when the load capacitance discharging circuit 18 is not provided.

On the other hand, when the on/off control signal ON is at "L" level and the discharging control signal DCG is at "H" level, the AND gate AD1 outputs a "H" level signal and thus the transistor TR13 is turned on. Accordingly, in this case, the output voltage VO1 of the DC/DC apparatus is rapidly lowered to 0V without depending on the load thereof since the charges corresponding to the output voltage are discharged through the transistor TR13.

The above will be explained with reference to Fig. 21.

When the on/off control signal ON is made "H" level at a point of time T0, the operation of the DC/DC apparatus is started. Accordingly, the voltage of the capacitor C125 gradually rises and reaches the same voltage as the reference voltage E1 at a point of time T1.

The output voltage of the DC/DC apparatus also gradually rises and reaches the rated voltage VO1 at the point of time T1.

Next, when the on/off control signal ON is made "L" level at a point of time T2, the operation of the DC/DC apparatus is stopped. At this time, the output end (VO1) of the DC/DC apparatus is short-circuited to the ground by the transistor TR13 and thus the charges corresponding to the load capacitance are forcibly discharged. As a result, the output voltage VO1 of the DC/DC apparatus reaches 0V at a point of time T3.

Contrary to this, the prior art DC/DC apparatus is not provided with the above load capacitance discharging circuit 18. Accordingly, as shown by broken lines in Fig. 21, the off time required until the output voltage of the DC/DC apparatus reaches 0V differs between the case of light load and the case of heavy load. According

to the present embodiment, it is possible to make the off time constant without depending on lightness or heaviness of the load.

Figures 22a and 22b show the circuit constitution of an embodiment (DC/DC apparatus using a synchronous rectifying control) of the DC/DC apparatus according to the second aspect of the present invention.

Figure 22a shows the constitution of the entire DC/DC apparatus. In Fig. 22a, reference TR21 denotes a switching transistor which is turned on/off in response to an output DH of the DC/DC control circuit 200; reference L21 denotes a choke coil for converting an input voltage VI to an output voltage V01; reference D21 denotes a fly-wheel diode for releasing energy accumulated in the choke coil L21 when the transistor TR21 is in off state; reference R21 denotes a resistor for sensing current to be fed to the load from the present DC/DC apparatus; reference C21 denotes a smoothing capacitor; reference C22 denotes a soft start capacitor; and reference TR22 denotes a synchronous rectifying transistor which is turned on/off in response to an output DL of the DC/DC control circuit 200. The synchronous rectifying transistor TR22 is turned on when a voltage is applied across the diode D21 in the forward direction, and is turned off when a voltage is applied across the diode D21 in the reverse direction. The synchronous rectifying transistor TR22 has the function of releasing energy accumulated in the choke coil L21 when the switching transistor TR21 is in off state.

Figure 22b shows the constitution of the DC/DC control circuit 200. In Fig. 22b, references R3 and R4 each denote a resistor for dividing the output voltage V01 of the DC/DC apparatus; reference 21 denotes an error amplifier for amplifying a difference between the voltage divided by the resistors R3 and R4 and one of a plurality of reference voltages (in the illustrated example, a voltage of the capacitor C22 and a reference voltage E2);

reference 22 denotes a triangular wave oscillator for oscillating a triangular wave signal at a constant frequency; and reference 23 denotes a PWM comparator for controlling an on period of its output pulse according to an output voltage of the error amplifier 21. The PWM comparator 23 compares a voltage of the triangular wave signal from the oscillator 22 with the output voltage of the error amplifier 21, and is brought to on state (or off state) when the voltage of the triangular wave signal is lower (or higher) than the output voltage of the error amplifier 21.

Also, reference IV2 denotes an inverter responsive to the on/off control signal ON; reference AD2 denotes an AND gate responsive to an output of the inverter IV2 and the discharging control signal DCG; reference EA denotes an error amplifier for detecting a voltage difference across the current sense resistor R21; and reference 25 denotes a synchronous rectifying control circuit responsive to an output of the error amplifier EA and an output of the PWM comparator 23. The synchronous rectifying control circuit 25 outputs a "H" level signal when the PWM comparator 23 is in off state and the output of the error amplifier EA is below a predetermined level.

Also, reference 28 denotes a charge pumping circuit for generating voltages necessary to turn on the switching transistor TR21 and the synchronous rectifying transistor TR22; reference OR1 denotes an OR gate responsive to an output of the synchronous rectifying control circuit 25 and an output of the AND gate AD2; reference 24 denotes a driver for turning on the switching transistor TR21 based on the voltage generated by the charge pumping circuit 28 when the PWM comparator 23 is in on state; and reference 26 denotes a driver for turning on the synchronous rectifying transistor TR22 in response to an output of the OR gate OR1.

Also, reference 29 denotes a power supply unit which responds to the on/off control signal ON and controls

on/off of the power supply to the DC/DC control circuit 200 to thereby control on/off (start/stop of the operation) of the entire DC/DC apparatus. Also, reference TR14 denotes a transistor for discharging charges of the capacitor C22 to set the terminal voltage thereof to 0 V when the operation of the DC/DC apparatus is stopped; and reference I2 denotes a constant current source for charging the capacitor C22 to raise the terminal voltage thereof in a constant time when the transistor TR14 is in off state.

Hereinafter, the explanation as to the load capacitance discharging control circuit constituted by the inverter IV2, the AND gate AD2 and the OR gate OR1 will be given.

In Fig. 22b, the DC/DC control circuit 200 starts its operation when the on/off control signal ON is at "H" level, and stops its operation when the on/off control signal ON is at "L" level. Also, the load capacitance discharging function is validated when the discharging control signal DCG is at "H" level, and is invalidated when the discharging control signal DCG is at "L" level.

When the on/off control signal ON is at "H" level, the inverter IV2 outputs a "L" level signal and thus the AND gate AD2 outputs a "L" level signal. Accordingly, the OR gate OR1 outputs the output signal of the synchronous rectifying control circuit 25 to the driver 26. As a result, no influence is exerted on the operation of the entire DC/DC control circuit 200.

Also, when the on/off control signal ON is at "L" level and the discharging control signal DCG is at "L" level, the AND gate AD2 outputs a "L" level signal. Accordingly, the OR gate OR1 outputs the output signal of the synchronous rectifying control circuit 25 to the driver 26. As a result, no influence is exerted on the operation of the entire DC/DC control circuit 200.

On the other hand, when the on/off control signal ON is at "L" level and the discharging control signal DCG is

at "H" level, the AND gate AD2 outputs a "H" level signal and thus the OR gate OR1 outputs a "H" level signal. As a result, the driver 26 is enabled to turn on the synchronous rectifying transistor TR22. When the transistor TR22 is turned on, the output end of the DC/DC apparatus is short-circuited via the transistor TR22 to the ground and thus the charges corresponding to the load capacitance are forcibly discharged. Therefore, it is possible to lower the output voltage of the DC/DC apparatus to OV in a substantially constant time, without depending on lightness or heaviness of the load of the DC/DC apparatus.

Figure 23 shows the circuit constitution by which turn-on/turn-off sequences are controlled between the two power supplies (the DC/DC apparatuses DC1 and DC2), and Fig. 24 shows the rise/fall characteristics of the output voltages based on the circuit constitution.

In Fig. 23, the constitution of each of the DC/DC apparatuses DC1 and DC2 is the same as that of the DC/DC apparatus shown in Fig. 22a.

The power turn-on sequence control with respect to the DC/DC apparatuses DC1 and DC2 is as explained with reference to Fig. 16. Namely, the respective rise characteristics of the output voltages VO1 and VO2 of the DC/DC apparatuses DC1 and DC2 are determined by the respective capacitances of the capacitors C221 and C222 without depending on lightness or heaviness of the corresponding loads.

Accordingly, for example, where the power supply to the DC/DC apparatus DC1 is first turned on and the power supply to the DC/DC apparatus DC2 is then turned on, such a power turn-on sequence can be realized by setting the capacitance of the capacitor C221 to be smaller than that of the capacitor C222.

Also, the power turn-off sequence control with respect to the DC/DC apparatuses DC1 and DC2 is as explained with reference to Figs. 22a and 22b.

The above will be explained with reference to Fig. 24.

The on/off control signal ON is commonly input to the DC/DC apparatuses DC1 and DC2 so as to simultaneously turn on the respective power supplies thereof. The discharging control signal DCG is also commonly input to the DC/DC apparatuses DC1 and DC2 and is set to "H" level.

The capacitance of the capacitor C221 is selected so that the output voltage of the DC/DC apparatus DC1 reaches the rated voltage VO1 at a point of time T1, and the capacitance of the capacitor C222 is selected so that the output voltage of the DC/DC apparatus DC2 reaches the rated voltage VO2 at a point of time T2.

When the on/off control signal ON is at "L" level, the respective operations of the DC/DC apparatuses DC1 and DC2 are stopped. When the on/off control signal ON is made "H" level at the point of time T0, the respective power turn-on sequences of the DC/DC apparatuses DC1 and DC2 are simultaneously started. Accordingly, the output voltage of the DC/DC apparatus DC1 reaches the rated voltage VO1 at the point of time T1, depending on the capacitance of the capacitor C221, and the output voltage of the DC/DC apparatus DC2 reaches the rated voltage VO2 at the point of time T2, depending on the capacitance of the capacitor C222.

Next, when the on/off control signal ON is changed from "H" level to "L" level at the point of time T3, the respective operations of the DC/DC apparatuses DC1 and DC2 are simultaneously stopped. At this time, the discharging control signal DCG is at "H" level and thus the respective synchronous rectifying transistors TR221 and TR222 are turned on. As a result, the respective output ends of the DC/DC apparatuses DC1 and DC2 are short-circuited to the ground and thus the charges corresponding to the respective load capacitances are forcibly discharged.

Thus, the output voltage of the DC/DC apparatus DC1 and the output voltage of the DC/DC apparatus DC2 can

simultaneously reach 0V at the point of time T4.

Figure 25 shows the circuit constitution by which the two power supplies (the DC/DC apparatuses DC3 and DC4) are simultaneously turned on/off, and Fig. 26 shows the
5 rise/fall characteristics of the output voltages based on the circuit constitution.

In Fig. 25, the on/off control signal ON is commonly input to the DC/DC apparatuses DC3 and DC4 so as to simultaneously turn on the respective power supplies
10 thereof. The discharging control signal DCG is also commonly input to the DC/DC apparatuses DC3 and DC4 and is set to "H" level.

When the on/off control signal ON is at "L" level, the respective operations of the DC/DC apparatuses DC3 and DC4 are stopped. When the on/off control signal ON is
15 made "H" level, the respective power turn-on sequences of the DC/DC apparatuses DC3 and DC4 are simultaneously started. At this time, since the capacitor C223 is commonly connected to the DC/DC apparatuses DC3 and DC4, the reference voltage (i.e., voltage of the capacitor
20 C223) of the DC/DC apparatus DC3 and the reference voltage (i.e., voltage of the capacitor C223) of the DC/DC apparatus DC4 begin to rise simultaneously and, after a lapse of certain time, reach the same voltage as the
25 reference voltage E2 simultaneously.

The above will be explained with reference to Fig. 26.

When the on/off control signal ON is made "H" level at a point of time T0, the respective operations of the DC/DC apparatuses DC3 and DC4 are started. Accordingly,
30 the voltage of the capacitor C223 gradually rises and reaches the same voltage as the reference voltage E2 at a point of time T1. The output voltage of the DC/DC apparatus DC3 also gradually rises and reaches the rated voltage VO3 at the point of time T1, and the output
35 voltage of the DC/DC apparatus DC4 also gradually rises and reaches the rated voltage VO4 at the point of time T1.

Next, when the on/off control signal ON is changed

from "H" level to "L" level at the point of time T2, the
respective operations of the DC/DC apparatuses DC3 and
DC4 are simultaneously stopped. At this time, the
discharging control signal DCG is at "H" level and thus
5 the respective synchronous rectifying transistors TR223
and TR224 are turned on. As a result, the respective
output ends of the DC/DC apparatuses DC3 and DC4 are
short-circuited to the ground and thus the charges
corresponding to the respective load capacitances are
10 forcibly discharged.

Thus, the output voltage of the DC/DC apparatus DC3
and the output voltage of the DC/DC apparatus DC4 can
simultaneously reach 0V at the point of time T3.

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